Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 91426

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019
Seventh Semester
Electronics and Communication Engineering
EC 6009 – ADVANCED COMPUTER ARCHITECTURE
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. How is Harvard Architecture better over Von Neumann architecture ?
2. What is influence of clock rate and cycles per instruction in CPU function ?
3. Compare hardware and software parallelism.
4. List one advantage and disadvantage for microprogrammed control.
5. Data parallelism tasks need not take equal time to execute. Justify.
6. Why does circuit switching effectively help in SIMD computers ?
7. Compare process and thread.
8. Why implicit parallel programming considered easier than explicit type ?
9. What is advantage of interrupt prioritizing in processors ?
10. What is Cache coherence and Cache updating ?

PART – B **(13×5=65 Marks)**

11. a) Write briefly on functioning of CPU while (i) fetching a word from memory and (ii) performance with reduced power consumption. **(7+6)**

(OR)

b) With block diagram, explain Flynns classification of computer architectures. **(13)**

12. a) Justify why : **(7+6)**
    i) thread level parallelism has better performance than instruction level parallelism.
    ii) single thread processors are slower than multi thread processors.

    (OR)

    b) Write briefly on the following : **(7+6)**
    i) Need for high speed computing
    ii) Dynamic branch prediction.

13. a) Explain the advantages of loop level parallelism with suitable example. **(13)**

    (OR)

    b) Write briefly on the following: **(7+6)**
    i) Architectural configuration of SIMD model
    ii) Sorting in parallel.

14. a) Write briefly on Latency, avoidance, reduction and hiding mechanisms in a multithreaded architecture.

    (OR)

    b) i) Compare briefly on the performances of shared and distributed memory architectures and
    ii) Justify on which of these have improved synchronization and memory consistency. **(7+6)**

15. a) Explain for memory management scheme briefly the (i) memory mapping (ii) cache performance. **(7+6)**

    (OR)

    b) Write briefly on the following: **(7+6)**
    i) RAID ii) Memory buses.

PART – C **(1×15=15 Marks)**

16. a) Design of a Arithmetic Logic Unit with hardwired control and microprogrammed control features for a processor. **(15)**

    (OR)

    b) A program is run on a 40 MHz CPU with instruction mix and corresponding count is as given below. Determine the Effective CPI, Execution time, MIPS rate of program. **(15)**

Instruction type	Clock cycle count	Instruction count
Integer atithmetic	1	45000
Floating point	2	32000
Data transfer	2	15000
Control transfer	2	8000